Redefining Measurement

ID900 Time Controller

Time-tagging, Delay Generation and Pattern Generation

IDQ's Time Controller is designed for flexibility and it aims to efficiently and reliably solve a large number of problems encountered in the modern laboratory. It performs the funtions of a number of devices: Time-tagger, delay generator, pattern generator, counter and discriminator. Its hardware consists of 4 inputs and 4 outputs that are interconnected internally via a fast FPGA. It offers two modes. The high speed mode allows fast count rates up to 100 Mcps on each channel and a binning of 100 ps while the high resolution mode has a binning of 13 ps and allows a maximum count rate of 25 Mcps on each of the four channels. The Time Controller is an evolutive device. Extra functionalities can be implemented remotely by updating the firmware and the software .

Key Features

- Time-tagging and histogramming
- Internal timestamps processing (coincidence, filters,etc...)
- Delay generation with multi-hit ability
- Pattern generation
- High-speed counter
- High precision discriminator (-2 V to +2 V in 1 mV steps)
- 4 input channels
- 4 output channels (NIM + LVTTL)
- High resolution mode: 8 ps RMS (20 ps FWHM) jitter and 13 ps bin width
- 1 GHz counters

Applications

- Time correlated single-photon counting (TCSPC)
- Fluorescence lifetime imaging
- LIDAR
- OTDR
- Quantum communication
- Quantum computing
- Material science

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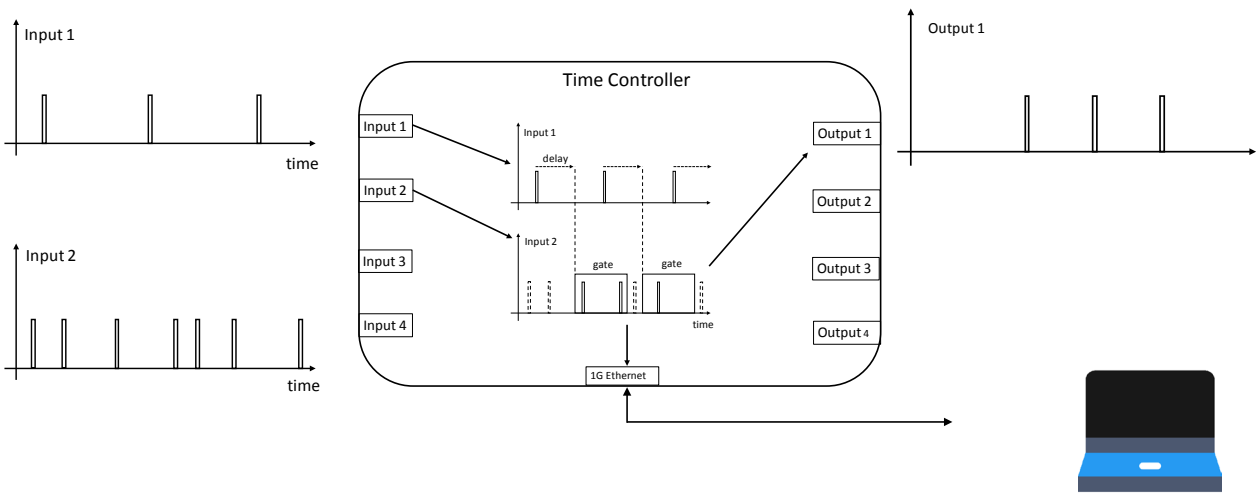
TIME CONTROLLER

Principle of Operation

The spirit of the Time Controller is to allow the user to perform the maximum amount of logical operation inside the device. It avoids heavy data processing on the computer and moreover offers the capability to generate conditionnal output signals to be sent back to the experimental setup (e.g control of an optical switch or of a detection gate).
We present below an example of the Time Controller usage. Here events coming from the input 1 pass through a temporal gate which is controlled by the events of input 2.



Specifications

Parameter	High Speed mode	High Resolution mode	Units
Input channel number	4 + Start	4	
Output channel number	4	4	
Bin width	100	13	ps
Time jitter (RMS)	<100	8	ps
Maximum processing rate (per channel)	100	25	Mevents/s
Maximum transfer rate to PC	10*	10*	Mevents/s
Maximum delay generation (typical)	1	1	ms
Output delay steps	100	100	ps
Counters speed	1	1	GHz
Discriminator range	-2 to 2	-2 to 2	V
Discriminator steps	1	1	mV

* Hardware ready for 100 Mcps

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